

## A HIGHLY RELIABLE 16 OUTPUT HIGH VOLTAGE NMOS/CMOS LOGIC IC WITH SHIELDED SOURCE STRUCTURE

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### ABSTRACT

A high voltage MOS IC, which consists of 16 high voltage NMOS transistor array having 400 V, 0.5 A output characteristic and its control CMOS logic, was newly developed. High and low voltage NMOS transistors of the IC are equipped with shielded source structure to realize completely parasitic bipolar effect-free high voltage MOS ICs.

Practically, this IC successfully drove a plasma display panel at 200 V, 2 MHz without any parasitic effect and its high operation reliability was verified.

To examine high integration density possibility, parasitic bipolar effects due to the interferences between high and high voltage transistors, low and low voltage transistors, and high and low voltage transistors, were experimentally investigated. As a result, it was confirmed that the "shielded source structure" realizes high density high voltage MOS ICs.

### INTRODUCTION

Recently, the cost and size reduction, and display area enlargement of flat display panels, such as PDP, ELD and dot matrix VFD, have been strongly demanded. Driver circuits for these display panels, necessarily have a lot of high voltage circuit outputs. Therefore, the monolithic IC equipped with high voltage transistors and their control logic circuits on the same chip, is essential to meet the above requirement. High voltage planar MOS ICs are thought to be most suited for such an IC, because of its isolation ease and high speed operation.<sup>[1-3]</sup>

However, negative resistance breakdown due to parasitic bipolar effect, is known to be observed in a high voltage planar NMOS transistor, a key device for high voltage MOS ICs.<sup>[4]</sup> Therefore, the high voltage transistor has a narrow ASO (Area of Safe Operation). To solve this problem, a high voltage MOS transistor with parasitic effect-free characteristic, was realized using the proposed "shielded source structure".<sup>[5][6]</sup>

The low voltage logic, for controlling the high voltage transistors, should be CMOS with low power dissipation and large noise immunity characteristic. However, since high resistivity substrate is used to realize high breakdown voltage for the high voltage MOS transistor, latch up phenomena in CMOS logic become easily to occur. Since the latch up is one of parasitic bipolar effect, the shielded source structure will be effective to suppress the latch up.

This paper describes, a newly developed, 16 output high voltage NMOS/CMOS logic IC without any parasitic effect. This is achieved by adopting shielded source structure. The possibility of realizing even higher integration density IC by using the shielded source structure is also discussed, based on experimental results.

### DEVICE STRUCTURE

In the new IC, the shielded source structure, in which the high impurity density p<sup>+</sup> ground layer entirely covers n<sup>+</sup> source layer except for the MOS channel plane, is adopted in high voltage NMOS transistors and in low voltage NMOS transistors for CMOS logic, as shown in Fig. 1. Since p<sup>+</sup> ground layer potential is equal to that for the source (n<sup>+</sup>), even if voltage drop at the substrate due to substrate current occurs, the source junction is not forward-biased. In consequence, the parasitic bipolar effect doesn't occur. These n<sup>+</sup> source layer and underlying p<sup>+</sup> ground layer are simply fabricated by As<sup>+</sup> and B<sup>+</sup> ion implantations through the same source mask windows in a self-aligned manner.

The IC is made up of 8 input-output buffer circuits, 16 blocks of serial-in/parallel-out shift register, latch, gate and buffer circuit and 16 output high voltage NMOS transistors (Fig. 2). The buffer circuit consisting of 4 stage inverters is designed to have 5 MHz driving capability for the high voltage transistor gate. The high voltage transistors are controlled by Output Enable (OE), Toggle (To) and Data (D in1 or D in2) input signals. The CMOS logic includes about 700 low voltage MOS transistors.

### EXPERIMENTAL RESULTS

A photomicrograph of the IC is shown in Fig. 3. IC chip size is 6 mm x 6 mm. The IC electrical characteristics are shown in Table 1. High voltage NMOS transistors having 4  $\mu$ m long, 10.2 mm wide MOS channel and 40  $\mu$ m long offset gate, can flow 0.5 A drain current at 10 V gate bias, which is a high enough current level to drive a large display area dot matrix AC refresh PDP. The high voltage transistor shows about 400 V drain breakdown voltage in the 0 V to 15 V wide gate bias range without any negative resistance, according to pulse current-voltage measurement. This characteristic is still superior to that for 100-150  $\mu$ m long offset gate conventional NMOS transistors. The conventional transistors have larger on-resistance and larger chip

occupation area compared to that for the shielded source transistor. Therefore, this structure enables easily realizing high integration density MOS ICs. Drain current-voltage characteristics for the high voltage shielded source transistor are shown in Fig. 4.

CMOS logic with shielded source structure (about 4  $\mu\text{m}$  gate length) operates at 2-30 V power supply voltage range and follows 9 MHz clock frequency at 10 V (Fig. 5) (5-6 MHz clock frequency will be large enough for about 2000 character AC refresh PDP to be driven). CMOS logic power consumption is 21 mW at 10 V, 5 MHz clock frequency, which is much less than the power consumption for an E/D MOS logic (over 100 mW).

If integration density increases further, there is a possibility that logic error operation due to a capacitive coupling noise pulse would occur. By using CMOS configuration in logic, stable logic operation is expected to be obtained due to its large noise margin. The other possibility is that the interferences between high and high voltage transistors, high and low voltage transistors, and low and low voltage transistors due to a substrate current, would occur. The substrate current will be caused by low and high voltage transistor's avalanche phenomena, p-n junction's (for example, drain junction for CMOS logic) forward-biasing resulting from capacitive coupling noise pulse and surge voltage.

For example, a large quantity of electrons injected into the substrate diffuse to a certain high voltage transistor and are likely to lead this transistor to negative resistance breakdown by causing the parasitic bipolar transistor to turn on. To investigate such a parasitic bipolar effect, the following experiment was made. In a high voltage transistor biased at a lower voltage than its breakdown voltage, electrons are injected from an adjacent high voltage transistor's drain junction into the substrate, by forward-biasing. These electrons enter into the transistor drain depletion layer and cause avalanche breakdown. As a result, a large quantity of holes are injected into the substrate and cause voltage drop at the substrate. According to the experiment, a conventional transistor showed parasitic bipolar action in low injection current in spite of at lower electric field than that of breakdown, whereas the shielded source transistor didn't show negative resistance breakdown, even at experimentally observable 450 mA injection current level.

Also, there is a possibility that latch up might occur in CMOS logic due to the substrate current. Since high voltage MOS IC uses high resistivity substrate, parasitic lateral npn transistor's base resistance, or the substrate resistance, is high, as mentioned previously. Therefore, when the substrate current causes enough voltage drop at the substrate resistance to make n-channel transistor source junction forward-bias, latch up occurs. In order to investigate such a parasitic bipolar effect, CMOS ability to withstand latch up was experimented upon. The conventional CMOS with 20  $\mu\text{m}$  parasitic lateral npn transistor base (p<sup>+</sup> substrate:  $N_A = 6 \times 10^{14} \text{ cm}^{-3}$ ) width  $L_M$ , results in latch up phenomena, as shown in Fig. 6; at 6 mA parasitic vertical npn transistor base (n-well region) injection current level, 10 V collector-emitter bias voltage. As compared with this characteristic, the CMOS with shielded source structure doesn't show latch up, even at 300-350 mA base injection current level. The reason is

that current gain  $\alpha_n$  for the parasitic npn transistor in the shielded source structure is less than  $3 \times 10^{-7}$ . These experimental investigations show that higher integration density IC will be realized.

The fabricated ICs in 28 pin ceramic packages were applied in a plasma display scan driver. The ICs successfully drove the panel at 200 V, 2 MHz without any parasitic effect and any logic operation error due to a capacitive coupling noise pulse (Fig. 7). As a result, in a practically usable high voltage IC, since parasitic bipolar action was effectively suppressed by using the shielded source structure, the high IC reliability was confirmed.

## CONCLUSION

A 16 output high voltage NMOS/CMOS logic IC, designed for driving an AC refresh PDP, was developed using shielded source structure for its NMOS transistors, to realize completely parasitic effect-free high voltage MOS ICs.

Practically, the IC succeeded in driving an AC refresh PDP and its high reliability was verified.

Parasitic effects due to the interferences between high and high voltage transistors, low and high voltage transistors, and low and low voltage transistors in this IC, were experimentally investigated.

These results indicate that much higher packing density, but still a parasitic effect-free high voltage NMOS/CMOS logic IC, will be realized using shielded source structure.

## ACKNOWLEDGEMENT

The authors wish to thank Drs. K. Ayaki and H. Kato for their continuous encouragement and T. Aizawa and K. Hirata for their technical assistance.

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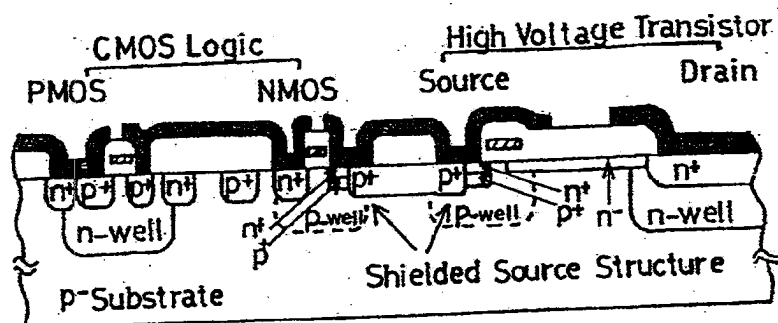


Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper n<sup>+</sup> source layer entirely shielded by a lower p<sup>+</sup> ground layer.

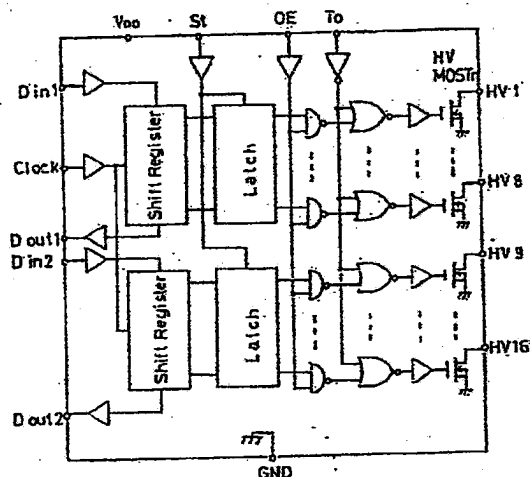


Fig.2 16 output high voltage MOS IC block diagram. Logic circuit is composed of serial-in and parallel-out shift registers, latches, gates and buffers.

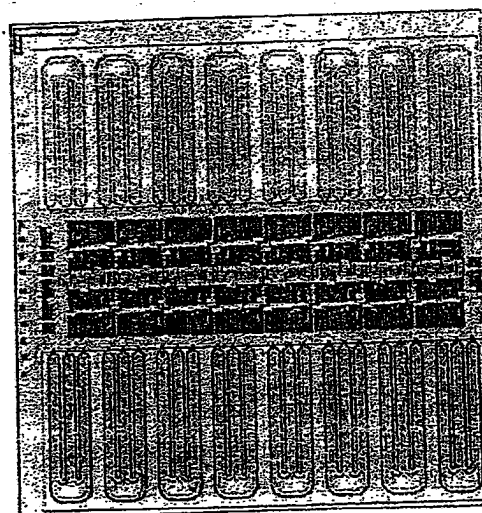


Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

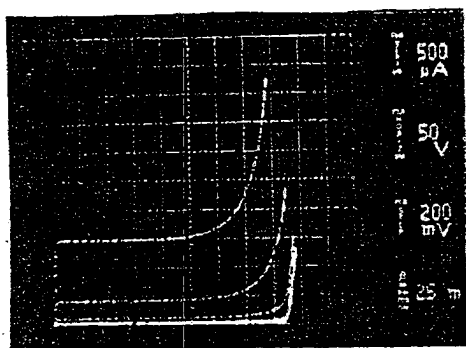


Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

High Voltage MOS Tr	
$BV_{oss}$ (at $I_D < 100 \mu A$ )	400 V
$R_{on}$ (at $V_G = 10 V$ )	$30 \Omega$
$I_{os}$ (at $V_G = 10 V$ )	0.5 A
Low Voltage Logic Circuit	
$f_{clock \max}$ (at $V_{DD} = 10 V$ )	9 MHz
$V_{DD}$	2V ~ 30V
$P_o$ (at $V_{DD} = 10 V$ , $f_{clock} = 5 MHz$ , $C_L = 15 pF$ )	21 mw

Table 1 Typical 16 output high voltage MOS IC characteristics. CMOS logic circuit can operate in wide power supply voltage range. High voltage NMOS transistor doesn't show any parasitic bipolar effect for wide gate bias range from 0 V to 15 V.

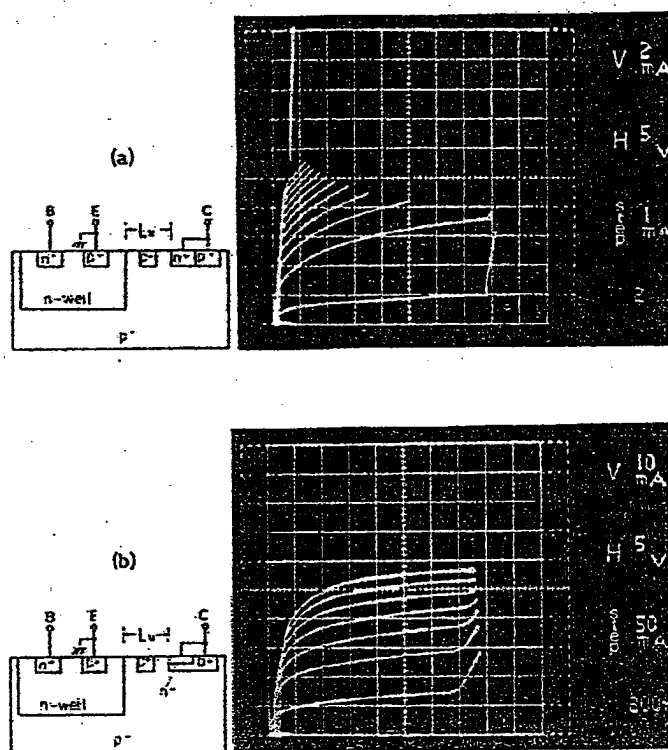


Fig.6 Base noise current at latch up. (a) For conventional CMOS. (b) For CMOS with shielded source structure. Conventional CMOS shows latch up at 6 mA base injection current level, 10 V collector-emitter bias voltage, whereas CMOS with shielded source structure doesn't show latch up phenomena, even at 350-400 mA.

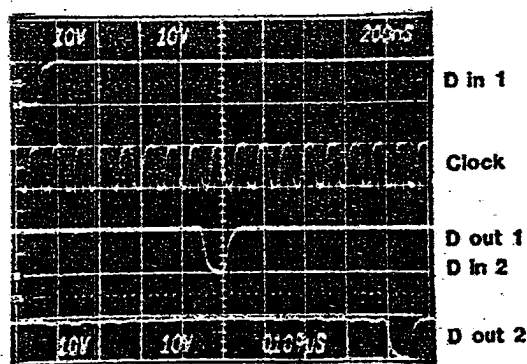


Fig.5 16 stage shift register's input and output waveforms at 9 MHz clock frequency, 10 V. Shift registers operate up to 12 MHz, at 20 V.

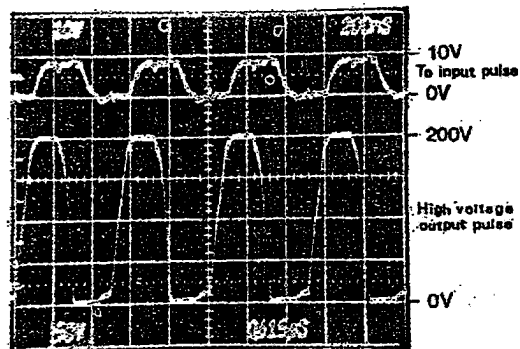


Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.



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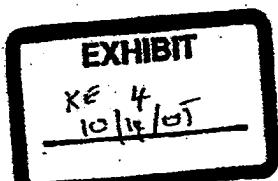
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## CONCLUSION

A 16 output high voltage NMOS/CMOS logic IC, designed for driving an AC refresh PDP, was developed using shielded source structure for its NMOS transistors, to realize completely parasitic effect-free high voltage MOS ICs.

Practically, the IC succeeded in driving an AC refresh PDP and its high reliability was verified.

Parasitic effects due to the interferences between high and high voltage transistors, low and high voltage transistors, and low and low voltage transistors in this IC, were experimentally investigated.

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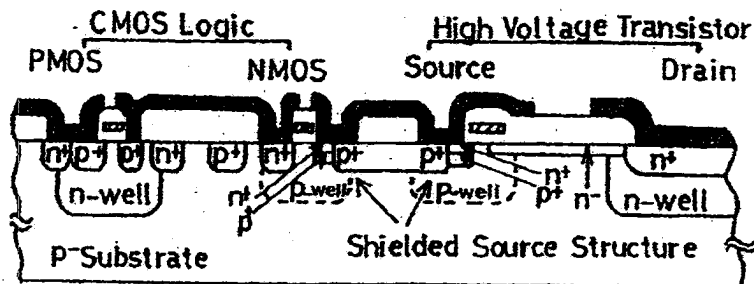


Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper n<sup>+</sup> source layer entirely shielded by a lower p<sup>+</sup> ground layer.

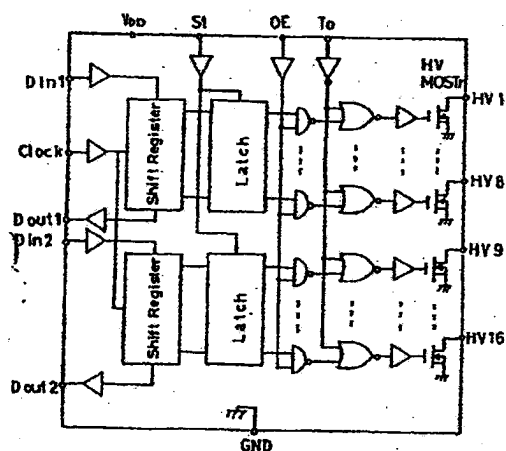


Fig.2 16 output high voltage MOS IC block diagram. Logic circuit is composed of serial-in and parallel-out shift registers, latches, gates and buffers.

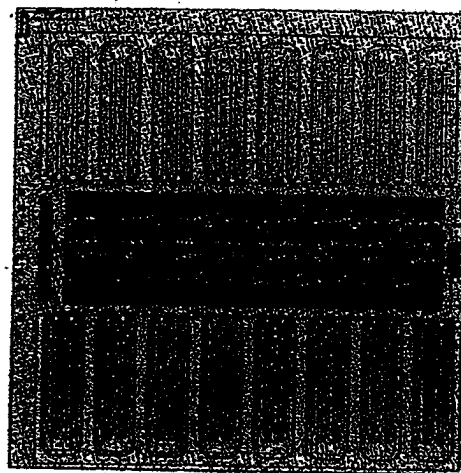


Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

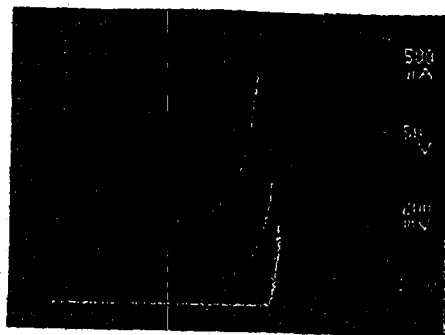


Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

High Voltage MOS Tr	
BV <sub>DS</sub> (at I <sub>D</sub> < 100 $\mu$ A)	400 V
R <sub>on</sub> (at V <sub>G</sub> = 10 V)	30 $\Omega$
I <sub>DS</sub> (at V <sub>G</sub> = 10 V)	0.5 A
Low Voltage Logic Circuit	
f <sub>clock</sub> max (at V <sub>DD</sub> = 10 V)	9 MHz
V <sub>DD</sub>	2 V ~ 30 V
P <sub>o</sub> (at V <sub>DD</sub> = 10 V, f <sub>clock</sub> = 5 MHz, C <sub>L</sub> = 15 pF)	21 mW

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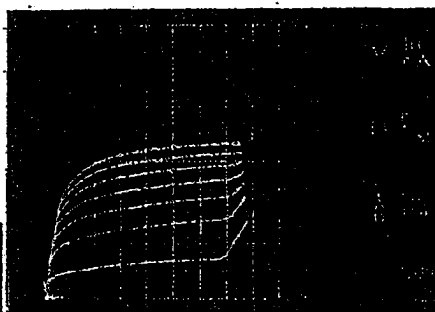
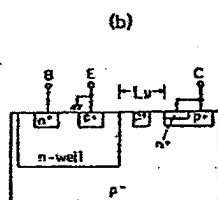
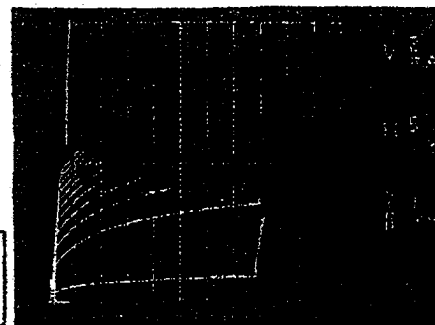
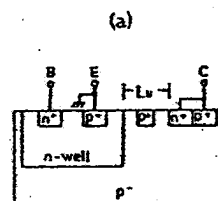


Fig.6 Base noise current at latch up. (a) For conventional CMOS. (b) For CMOS with shielded source structure. Conventional CMOS shows latch up at 6 mA base injection current level, 10 V collector-emitter bias voltage, whereas CMOS with shielded source structure doesn't show latch up phenomena, even at 350-400 mA.

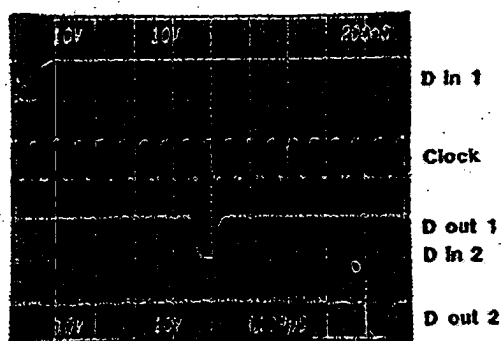


Fig.5 16 stage shift register's input and output waveforms at 9 MHz clock frequency, 10 V. Shift registers operate up to 12 MHz, at 20 V.

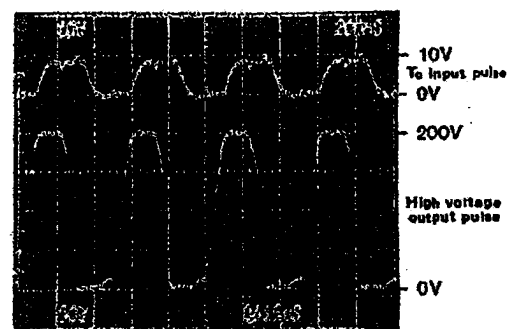
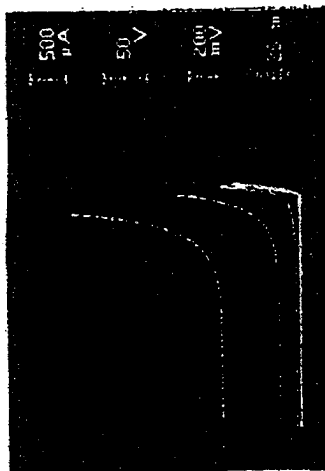


Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.





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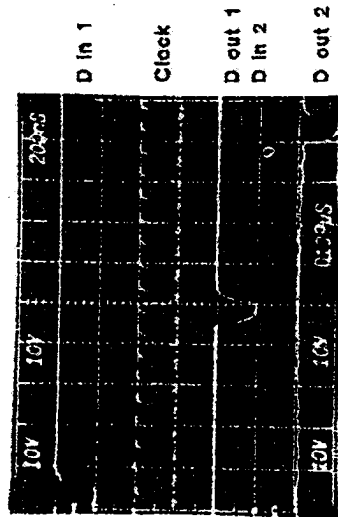


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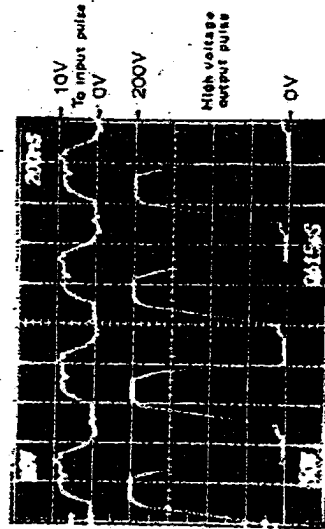


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## WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN

Welcome to the 1982 International Electron Devices Meeting, the international forum for the presentation of latest results of research and development in electron devices! For the first time this meeting is being held in San Francisco in response to the growing geographical base of IEDM participation. In the future the location of the IEDM will alternate between Washington, D.C. and San Francisco.

This meeting, in its 28th year, has and continues to reflect the dramatic growth and pervasiveness of a broad spectrum of electron devices. It has provided the setting for both the exchange and birth of new ideas fueling electronics progress. Both the technical and the international breadth of this conference are evidenced by the program this year which contains 188 contributed papers selected from the 425 submitted abstracts from 17 countries around the world. These papers comprise 29 sessions in six major categories: Solid State Devices; Detectors, Sensors, and Displays; Quantum Electronics and Energy Conversion Devices; Device Technology; Integrated Circuits; and Electron Tubes. In addition, the three areas of Device Technologies for High Speed Logic, Integrated Power Devices, and Automation in Semiconductor Fabrication, are highlighted in the Plenary Session. These areas are further examined in four concurrent panel sessions Tuesday evening which cover: Bipolar and MOS Technology: Choices for VLSI Applications; the Silicon Foundry: Myth or Reality; High Voltage Integrated Circuits: Applications and Technology; and High-Speed Devices and Technology.

An emerging development made possible by the broad electronics progress in the last quarter century, and destined to have a major impact on our society, is the use of robots. The robotics revolution will be addressed by our Tuesday luncheon speaker, Dr. David Nit-zan, Director of Robotics Development at SRI International.

I congratulate the Conference Committee for the outstanding job they have done in planning and organizing the 1982 IEDM, and on behalf of the IEEE Electron Devices Society, which sponsors the IEDM, I want to extend my sincere appreciation for their dedicated professional efforts. In addition, the authors are to be commended for their efforts towards technical excellence in their papers. It is with pleasure that I welcome them and all attendees to the 1982 International Electron Devices Meeting.



Al F. Tasch, Jr.  
General Chairman



Michael Adler  
Technical Program  
Chairman

Al Tasch  
General Chairman

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- 1.2 INTEGRATED POWER DEVICES, J. Tihanyi, Siemens AG, Munich, GERMANY
- 1.3 AUTOMATION IN SEMICONDUCTOR MANUFACTURING, T. Makimoto and H. Nagatomo, Musashi Works, Hitachi, Ltd., Tokyo, JAPAN

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J. Dayton

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- 2.5 THREE OCTAVES WITH ONE TWT, J.F. Rymes, and M.J. Castone, Varian Associates, Incorporated, Palo Alto, CA

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- 2.6 GRIDDED PIERCE GUN DESIGN AND THE PAM FOCUSING OF BEAMS FROM GRIDDED ELECTRON GUNS, R. True, Litton Industries, San Carlos, CA

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- 2.7 A DIAGNOSTIC TECHNIQUE FOR EVALUATION OF CATHODE EMISSION PERFORMANCE AND DEFECTS IN VEHICLE ASSEMBLY, M.J. Castellino, G.V. Miram, and W.R. Ayers, Varian Associates, Incorporated, Palo Alto, CA

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- 3.2 RELIABILITY OF THIN SiO<sub>2</sub> FILMS SHOWING INTERDIGITAL DIELECTRIC INTEGRITY, Y. Hōkan, T. Baba, and N. Kawamura, Nippon Electric Company, Ltd., Kawasaki, JAPAN

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- 3.3 MOSFET DEGRADATION DUE TO STRESSING OF THIN OXIDE, M.S. Liang, Y.T. Yeow, C. Chang, C. Hu, and R.W. Bradders, University of California, Berkeley, CA

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- 3.4 INFLUENCE OF THE STATE OF POLYSILICON/SILICON DIOXIDE INTERFACE ON MOS PROPERTIES, N. Light, and S. Ebra, Bell Laboratories, Murray Hill, NJ

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- 3.5 AN ISOLATION TECHNOLOGY FOR HIGH PERFORMANCE BIPOLAR MEMORIES IOP-II, H. Goto, T. Takata, R. Aoki, Y. Kawabe, K. Dami, and M. Tanaka, Fujitsu Limited, Kawasaki, JAPAN

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- 3.6 U-GROOVE ISOLATION TECHNIQUE FOR HIGH SPEED BIPOLAR YESIS, A. Hayasaka, Y. Tamaki, and M. Kawamura, Hitachi, Ltd., Tokyo, JAPAN; K. Ogino, Device Development Center, Tokyo, JAPAN; and S. Ohwaki, Takasaki Works, Gumma, JAPAN

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W. Hunter

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S. Kohyama

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P.R. Senti

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M.C. Driver

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Y. Nishi

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H.S. Fo

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**SESSION 13: Quantum Electronics—III-V Heterostructure Photonic Devices**

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Co-Chairmen: R.W.H. Engelman  
R.E. Leheny

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10:45 a.m.

13.5 A GAIN-GUIDED STRIPE DIODE LASER WITH A SINGLE LONGITUDINAL MODE, HIGH KINK POWER, AND MINIMAL BEAM DISTORTION, R.W.H. Engelman, D. Kerps, G. Hom, and D.E. Asckley, *Hewlett-Packard Laboratories, Palo Alto, CA*

11:10 a.m.

13.6 HIGH POWER (600 mW CW) PHASE-LOCKED SEMICONDUCTOR LASER ARRAYS, D.R. Scifres, R.D. Burham, and W. Streifer, *Xerox Palo Alto Research Center, Palo Alto, CA*

11:35 a.m.

13.7 LOW THRESHOLD 1.3  $\mu$ m GaInAsP/InP BURIED OPTICAL WAVEGUIDE LASERS, W. Ng, C.L. Jiang, and P.D. Dapkus, *Rockwell International, Thousand Oaks, CA*

**SESSION 14: Electron Tubes—Gyrotrons and Gyro-TWTs**

Tuesday, December 14, 2:15 p.m.  
Continental Ballrooms 1,2,3

Co-Chairmen: N. Vanderplaat  
H. Jory

2:15 p.m.

**INTRODUCTION**

2:20 p.m.

14.1 DESIGN AND OPERATION OF MAGNETRON INJECTION GUNS FOR A 140 GHz GYROTRON, K. Felch, D. Stone, H. Jory, R. Garcia, and G. Wendell, *Varian Associates, Incorporated, Palo Alto, CA*, and R. Temkin and K. Kreischer, *Plasma Fusion Center, Massachusetts Institute of Technology, Cambridge, MA*

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2:45 p.m.  
14.2 250-KW HIGH-EFFICIENCY GYROTRON OSCILLATOR OPERATING AT 60 GHz, W. DeHope, P. Ferguson, V. Matanga, I. Saidoval, and J. Tancredi, Hughes Aircraft Company, Torrance, CA 366

3:10 p.m.  
14.3 DEVELOPMENT OF 21GHz-70GHz GYROTRONS, K. Sugimoto, K. Fujita, Toshiba Corporation, Kawasaki, JAPAN, Y. Terumitsu, S. Tanaka, Kyoto University, and T. Idehata, Fukui University 368

3:35 p.m.  
14.4 A HIGH-POWER COMPLEX-CAVITY GYROTRON FOR FUSION-RESEARCH DEVICES, Y. Carmel, University of Maryland, A.K. Ganguly, D. Diakakis, Science Applications, B. Seely, JYCOG, and M. Reid, K.K. Chu, J. Levine, V. Granatstein, Naval Research Lab., Washington, DC 372

4:00 p.m.  
14.5 A WIDEBAND FUNDAMENTAL MODE MILLIMETER GYROTRON TWA EXPERIMENT, L.R. Barnett, K.R. Chu, C.R. Kyle, V.I. Granatstein, Naval Research Laboratory, Washington, DC, and Y.Y. Lau, Science Applications Inc., McLean, VA 375

4:25 p.m.  
14.6 SELF-CONSISTENT NON-LINEAR THEORY OF TWT GYROTRON, A.K. Ganguly, and S.Y. Ahn, Naval Research Laboratory, Washington, DC 379

4:50 p.m.  
14.7 IMPEDANCE CALCULATIONS FOR TRAVELING-WAVE GYROTRONS OPERATING AT HARMONICS OF THE CYCLOTRON FREQUENCY IN CIRCULAR AND RECTANGULAR OVERMODED WAVEGUIDES, R.W. Grow, and R.B. Marks, University of Utah, Salt Lake City, UT 380

5:15 p.m.  
14.8 IMPEDANCE CALCULATIONS FOR TRAVELING-WAVE GYROTRONS OPERATING AT HARMONICS OF THE CYCLOTRON FREQUENCY IN MAGNETRON-TYPE CIRCUITS OPERATING IN THE  $\pi$  MODE, R.W. Grow, and G.A. Shrivastava, University of Utah, Salt Lake City, UT 384

#### SESSION 15: Device Technology—Lithography and Pattern Transfer

Tuesday, December 14, 2:15 p.m.  
Continental Ballrooms 4 & 5

Co-Chairmen: B. Grilling, R. Gurnann

2:15 p.m.  
INTRODUCTION

2:20 p.m.  
15.1 MODELS OF ETCHING IN PLASMAS AND BEAMS, (Invited Paper), T.M. Mayer, University of North Carolina, Chapel Hill, NC 389

2:45 p.m.  
15.2 MULTI-LAYER RESIST SYSTEMS AS A MEANS TO SUBMICRON OPTICAL LITHOGRAPHY, (Invited Paper), B.J. Lin, IBM T.J. Watson Research Center, Yorktown Heights, NY 391

3:00 p.m.  
15.3 NEW TRI-LEVEL STRUCTURES FOR SUB-MICRON PHOTOLITHOGRAPHY, S. Matsui and N. Endo, Nippon Electric Company, Ltd., Kawasaki, JAPAN 395

3:35 p.m.  
15.4 LINEWIDTH CONTROL USING ANTI-REFLECTIVE COATING FOR OPTICAL LITHOGRAPHY, Y.C. Lin, A.J. Purdes, S.A. Saller, and W.R. Hunter, Texas Instruments Incorporated, Dallas, TX 399

4:00 p.m.  
15.5 SUBMICRON MOS PROCESS WITH 100% OPTICAL PROJECTION PRINTING AND ANISOTROPIC DRY ETCHING, W. Arden, W. Beinvoigt, and W. Muller, Siemens Research Laboratories, München, WEST GERMANY 403

4:25 p.m.  
15.6 HIGH PRECISION LITHOGRAPHY FOR SUBMICRON LSI FABRICATION, T. Matsuda, K. Iwadate, S. Moriya, and K. Harada, Musashino Electrical Communication Lab., N.T.T., Tokyo, JAPAN 407

4:50 p.m.  
15.7 X-RAY LITHOGRAPHY SYSTEM FOR SUBMICRON DEVICE FABRICATION, B. Fay, A. Gornowicz, and J.P. Nivoliens, Thomson-CSF, Orsay, FRANCE 411

5:15 p.m.  
15.8 0.2 MICRON LENGTH MUSHROOM GATE FABRICATION USING A NEW SINGLE-LEVEL PHOTORESIST TECHNIQUE, P.C. Chao, W.H. Ku, Cornell University, Ithaca, NY, P.M. Smith, and W.H. Perkins, General Electric Company, Syracuse, NY 415

#### SESSION 16: Device Technology—Technologies for Silicon-on-Insulator Devices

Tuesday, December 14, 2:15 p.m.  
Continental Ballrooms 6, 7, & 8

Co-Chairmen: D.A. Antoniadis, H. Friedrich

2:15 p.m.  
INTRODUCTION

2:20 p.m.  
16.1 MOS TRANSISTORS IN BEAM-RECRYSTALLIZED POLYSILICON (Invited Paper), T. Kamins, Hewlett-Packard Laboratories, Palo Alto, CA 420

2:45 p.m.  
16.2 CHARACTERISTICS OF MOSFETS FABRICATED ON LASER-RECRYSTALLIZED SILICON ISLANDS ON AMORPHOUS SUBSTRATES USING SELECTIVE ABSORPTION AND BEAM-SHAPING TECHNIQUES, G.E. Pospisil, H.G. Parks, S.W. Chiang, and Y.S. Liu, General Electric Company, Schenectady, NY 424

3:10 p.m.  
16.3 CHARACTERISTICS OF MOS DEVICES IN ELECTRON BEAM-RECRYSTALLIZED SILICON ON INSULATOR, Y. Ohmura, K. Shibata, T. Inoue, T. Yoshii, and Y. Horike, Toshiba Corporation, Kawasaki, JAPAN 429

3:35 p.m.  
16.4 CHARACTERIZATION OF LASER-SOI DOUBLE-SI ACTIVE LAYERS BY FABRICATING ELEMENTARY STRUCTURES, T. Warabisako, M. Miyao, M. Ohkura, and T. Yokuyama, Hitachi, Ltd., Tokyo, JAPAN 433

4:00 p.m.  
16.5 DEVICE CHARACTERIZATION ON MONOCRYSTALLINE SILICON GROWN OVER SiO<sub>2</sub> BY ELO (EPITAXIAL LATERAL OVERGROWTH) PROCESS, A.C. Igzi, L. Jastrzebski, and J.F. Corboy, RCA Laboratories, Princeton, NJ 437

4:25 p.m.  
16.6 SOI CMOS CIRCUIT PERFORMANCE ON GRAPHITE STRIP HEATER RECRYSTALLIZED MATERIAL, S.D.S. Mahli, H.W. Lam, and R.F. Philzotta, Texas Instruments Incorporated, Dallas, TX 441

4:50 p.m.  
16.7 FIELD-EFFECT IN LARGE GRAIN POLYSILICON TRANSISTORS, J.P. Colinge, E. Demgouille, and H. Moriel, Centre National d'Etudes des Télécommunications, Meudon, FRANCE 444

# SESSION 17: Integrated Circuits— Scaled CMOS

Tuesday, December 14, 2:15 p.m.  
Imperial Room

Co-Chairmen: E.L. Eraser  
K. Kolkopon

2:15 p.m.

## INTRODUCTION

2:20 p.m.

17.1 REDUCED GEOMETRY CMOS TECHNOLOGY (Invited Paper), R. Jerdonet, M. Chizzo, J. Weaver, General Electric Company, Schenectady, NY, and S. Combs, Intel Corporation, Cupertino, CA

2:45 p.m.

17.2 CHARACTERIZATION OF CMOS LATCH-UP, C.C. Hoang, M.D. Hartruff, N.F. Pu, C. Yue, C. Rahn, J. Schrankler, G.D. Kirchner, E.L. Hampton, and T.E. Henrichsen, Honeywell Incorporated, Plymouth, MN

3:10 p.m.

17.3 SURFACE INDUCED LATCH-UP IN VLSI CMOS CIRCUITS, D. Takacs, C. Werner, J. Harter, and U. Schwabe, Siemens AG, München, WEST GERMANY

3:35 p.m.

17.4 CMOS LATCH-UP ELIMINATION USING SCHOTTKY BARRIER EMOS, M. Sugino, Motorola, Phoenix, AZ, L.A. Akers, Arizona State University, Tempe, AZ, and M. Rebeschini, Motorola, Mesa, AZ

4:00 p.m.

17.5 LIGHTLY DOPED SCHOTTKY MOSFET, G.J. Koenke, and W.T. Lynch, Bell Laboratories, Murray Hill, NJ

4:25 p.m.

17.6 COUNTERDOPED WEL STRUCTURE FOR SCALED CMOS, K. Hashimoto, S. Morita, H. Nozawa, and S. Kohyama, Toshiba Corporation, Kawasaki, JAPAN

4:50 p.m.

17.7 A REDUCED SIZE CMOS SRAM CELL STRUCTURE WITH TWO-LEVEL AL INTERCONNECTION, O. Rudoh, I. Sakai, S. Murakami, and H. Yamamoto, Nippon Electric Company, LTD., Kanagawa, JAPAN

# SESSION 18: Solid State Devices—Discrete and Monolithic Bipolar Devices

Tuesday, December 14, 2:15 p.m.  
Hilton Plaza

Co-Chairmen: H. Strack  
H.N. Yu

2:15 p.m.

## INTRODUCTION

2:20 p.m.

18.1 NORMALLY-OFF TYPE HIGH SPEED Si-THYRISTOR, Y. Nakamura, H. Tadano, S. Sugiyama, I. Igarashi, Toyota Central Research and Development Labs., Incorporated, Aichi-ken, JAPAN, T. Ohmi, and J. Nishizawa, Tohoku University, Sendai, JAPAN

2:45 p.m.

18.2 A REGIONAL ANALYTIC MODEL FOR CURRENT INTERRUPTION IN HIGH VOLTAGE CENTER GATED BIPOLAR SWITCHES, J.E. Kohl, E.G. Gammel, A.R. Harman, M.D. Hirsch, T.J. Riley, and R.S. Scott, Bell Laboratories, Murray Hill, NJ, Reading, PA

3:10 p.m.

18.3 AN ANALYTICAL MODEL FOR THE FORWARD CHARACTERISTICS OF GATED P-I-N SWITCHES APPLIED TO LATERAL STRUCTURES, J.C. Gammel, H.W. Becke, M.A. Shihb, R.K. Smith, and Y.H. Wong, Bell Laboratories, Murray Hill, NJ, Reading, PA

3:35 p.m.

18.4 SWITCHING CHARACTERISTICS OF HIGH POWER BURIED GATE TURN-OFF THYRISTOR, T. Suzuki, T. Uezaki, M. Kikura, T. Watanabe, and T. Sueoka, Meiden-shu Electric Mfg. Co., Ltd., Osaka, JAPAN

4:00 p.m.

18.5 A TIME- AND TEMPERATURE-DEPENDENT SIMULATION OF THE GTO TURN-OFF PROCESS, A. Nakagawa, Toshiba Research and Development Center, Kawasaki, JAPAN, D.H. Navon, University of Massachusetts, Amherst, MA

4:25 p.m.

18.6 THE TOPOGRAPHY OF CURRENT DENSITY IN BIPOLAR TRANSISTORS, P.L. Howe, G.L. Martinelli, and S.A. Mittleman, Unirode Corporation, Watertown, MA

4:50 p.m.

18.7 A STUDY OF FORWARD SECOND-BREAKDOWN IN SILICON BIPOLAR POWER TRANSISTORS USING THE UNIT-CELL CONCEPT, R.U. MacInnell, RCA Laboratories, Princeton, NJ, G.E. Wicelley, Jr., and K.A. Sassaman, RCA Solid State Division, Mountaintop, PA

# SESSION 19: Quantum Electronics—Photovoltaic and Photoconductor Devices

Tuesday, December 14, 2:15 p.m.  
Franciscan Room

Co-Chairmen: P. Borden  
R. Schwartz

2:15 p.m.

## INTRODUCTION

2:20 p.m.

19.1 TWO DIMENSIONAL EFFECTS IN CONVENTIONAL SOLAR CELLS OPERATED AT HIGH INTENSITIES, J.E. Gray, R.J. Schwartz, Purdue University, West Lafayette, IN, and R.D. Nasby, R.D. Nasby, Sandia National Laboratories, Albuquerque, NM

2:45 p.m.

19.2 FABRICATION OF IMPROVED AND STABLE THIN FILM CIS-CUS SOLAR CELLS BY INHIBITING VERTICAL JUNCTION FORMATION, A.C. Rastogi, National Physical Laboratory, New Delhi, INDIA

3:10 p.m.

19.3 CHARACTERIZATION AND OPTIMIZATION OF AMORPHOUS SILICON SOLAR CELLS BY VARIATION OF DEVICE GEOMETRY, M.K. Han, W.A. Anderson, R. Lahri, and H. Wiesmann, State University of NY at Buffalo, Buffalo, NY

3:35 p.m.

19.4 GaAs SCHOTTKY PHOTODIODE WITH 3dB BANDWIDTH OF 20 GHz, S.Y. Wang, D.M. Bloom, and D.M. Collins, Hewlett-Packard Laboratories, Palo Alto, CA

4:00 p.m.

19.5 A 27 PICOSECOND PHOTODETECTOR WITH A MODULATION DOPED ALGa<sub>0.4</sub>As/GaAs HETERO-STRUCTURE, C.Y. Chen, C.G. Bethea, A.Y. Cho, P.A. Cardinelli, and B.F. Levine, Bell Laboratories, Murray Hill, NJ

4:25 p.m.

19.6 THE MICROWAVE MESFET OPTICAL DETECTOR, J.R. Forrest, F.P. Richards, University College London Torrington Place, London, and A. Perichon, Centre National d'Etudes des Telecommunications, Lannion, France

4:50 p.m.

19.7 SWITCHING DEVICE BASED ON THE QUANTUM HALL EFFECT, R.F. Kazarinov, and S. Luryi, Bell Laboratories, Murray Hill, NJ

**SESSION 20: Evening Panel Discussion**

Tuesday, December 14, 8:00-10:00 p.m.  
Continental Ballrooms 1,2,3,4

Panel Organizer: Joseph C. Logue  
IBM  
Yorktown Heights, New York

**THE SILICON FOUNDRY—MYTH OR REALITY?****PANEL DISCUSSION MEMBERS**

Panel Moderator: Joseph C. Logue  
IBM  
Yorktown Heights, New York

Allan Bell Xerox Palo Alto, CA	Peter Jones Intel Chandler, Arizona
Devin Buss Texas Instruments Dallas, Texas	Paul Low IBM Hopewell Junction, NY
Danny Cohen Cal Tech Marina Del Rey, CA	James Meindl Stanford University Stanford, CA
Robert Crosby IBM Foughkeepsie, NY	Gene Strull Westinghouse Baltimore, Maryland

**SESSION 21: Evening Panel Discussion**

Tuesday, December 14, 8:00-10:00 p.m.  
Continental Ballroom 3

Panel Organizer: Adrian Hartman  
Bell Laboratories  
Murray Hill, New Jersey

**HIGH-VOLTAGE INTEGRATED CIRCUITS—APPLICATIONS AND TECHNOLOGY****PANEL DISCUSSION MEMBERS**

Panel Moderator: Adrian R. Hartman Bell Laboratories Murray Hill, NJ	
Tom Englebos Texas Instruments Dallas, TX	Ran Ronen Xerox Corp. El Segundo, CA
Bernad Hoeflinger Univ. of Minnesota Minneapolis, MN	Ray Roop Motorola Inc. Phoenix, AZ
Keisuke Kataoka OKI Electric Industry Co. Tokyo, Japan	
James Mayrand Sprague Electric Co. Worcester, MA	Peter Shackle Harris Semiconductor Melbourne, FL

**SESSION 22: Evening Panel Discussion**

Tuesday, December 14, 8:00-10:00 p.m.  
Continental Ballroom 6

Panel Organizer: Richard Eden  
GigaBit Logic, Inc.  
Culver City, California

**HIGH-SPEED DEVICES AND TECHNOLOGY****PANEL DISCUSSION MEMBERS**

Panel Moderator: Richard C. Eden  
GigaBit Logic, Inc.  
Culver City, CA

Dexter Eastman Cornell University Ithaca, NY	Tushar R. Ghemwala IBM Yorktown Heights, NY
Herber Kroemer University of California Santa Barbara, CA	Nuyen T. Linh Thompson-CSF Orsay, France
R. Allen Murphy MIT Lincoln Laboratories Lexington, MA	Paul Solomon IBM Yorktown Heights, NY

**SESSION 23: Evening Panel Discussion**

Tuesday, December 14, 8:00-10:00 p.m.  
Imperial Room

Panel Organizer: Rick Davies  
Texas Instruments  
Dallas, Texas

**BIPOLAR AND MOS TECHNOLOGY: CHOICES FOR VLSI APPLICATIONS****Panel:**

Alan Anzai Hitachi Ltd.	Bill Herndon Fairchild Semiconductor
Harry Boll Bell Laboratories	F.M. Klaassen Phillips Research, Holland
Pallab Chatterjee Texas Instruments	Tak Ning IBM
Barry Dunbridge TRW	Jim Plummer Stanford University

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**SESSION 24: Device Technology—Advanced Interconnect Technologies**

Wednesday, December 15, 9:00 a.m.  
Continental Ballroom 4 & 5

Co-Chairmen: C. Parillo  
S. Minagawa

9:00 a.m.  
**INTRODUCTION**

9:05 a.m.  
24.1 MULTI-DIMENSIONAL SIMULATION OF VLSI WIRING CAPACITANCE (Invited Paper), F.E. Cottrell, E.M. Bittorf, and D.R. Thomas, IBM Corporation, Essex Junction, VT 548

9:30 a.m.  
24.2 ADVANCED PLANAR METALLIZATION WITH POLYMER FOR VLSI, T. Nishida, A. Saiki, Y. Homma, and K. Murai, Hitachi, Ltd., Tokyo JAPAN 552

9:55 a.m.  
24.3 LOW RESISTANCE MOS TECHNOLOGY USING SELF-ALIGNED REFRACTORY SILICIDATION, H. Okabayashi, E. Nagasawa, and M. Morimoto, Nippon Electric Company, Kawasaki, JAPAN 556

10:20 a.m.  
24.4 MO<sub>2</sub>N/MO GATE MOSFETS, M.J. Kim and D.M. Brown, General Electric Company, Schenectady, NY 560

10:45 a.m.  
24.5 MOLYBDENUM FILM PROPERTIES FOR SUBMICRON VLSI, H. Oikawa, T. Amazawa, and H. Kynagi, Nippon Telegraph and Telephone Public Corporation, Tokyo, JAPAN 564

11:10 a.m.  
24.6 LASER-ASSISTED POLY-SI RESISTOR FUSE UTILIZING SILICON LATERAL FLOW, T. Iwai, N. Sasaki, S. Kawamura, and M. Nakano, Fujitsu Limited, Kawasaki, JAPAN 568

11:35 a.m.  
24.7 ELECTRON-BEAM FUSE PROGRAMMING FOR REDUNDANCY TECHNOLOGY, K. Hashimoto, T. Takigawa, S. Morita, and S. Kohyama, Toshiba Corporation, Kawasaki, JAPAN 572

**SESSION 25: Solid State Devices—High-Speed III-V Devices**

Wednesday, December 15, 9:00 a.m.  
Continental Ballroom 6 & 7

Co-Chairmen: D.E. Askeley  
K. Hess

9:00 a.m.  
**INTRODUCTION**

9:05 a.m.  
25.1 MATERIAL AND DEVICE CONSIDERATIONS FOR SELECTIVELY DOPED HETEROJUNCTION TRANSISTORS (Invited Paper), J.V. DiLorenzo, R. Dingle, M. Feder, A.C. Gosard, R. Hendel, J.C.M. Hwang, A. Kaslalsky, V.E. Keramides, R.A. Kjel, and P. O'Connor Bell Laboratories, Murray Hill, NJ 578

9:30 a.m.  
25.2 HIGH SPEED LOW POWER GaAs/AlGaAs TEGFET INTEGRATED CIRCUIT, N.T. Linh, P.N. Tuong, D. Delagebeaudant, P. Delacuse, and M. Laviron, Thomson-CSF, Orsay, FRANCE 582

9:55 a.m.  
25.3 HIGH VELOCITY N-ON AND N-OFF MODULATION DOPED GaAs/AlGaAs FETs, T.J. Drummond, S.L. Su, W. Kopp, R. Fischer, R.E. Thorne, H. Morkoc, University of Illinois, Urbana, IL, K. Lee, and M.S. Shur, University of Minnesota, Minneapolis, MN 586

10:20 a.m.  
25.4 0.3 μm GATE LENGTH SUPER LOW NOISE GaAs MESFET, H. Ishiuchi, H. Mizuno, Y. Kaneko, K. Arai, and K. Suzuki, Nippon Electric Company, Ltd., Kawasaki, JAPAN 590

10:45 a.m.  
25.5 SUBMICRON GaAs VERTICAL ELECTRON TRANSISTOR, U. Mishra, L.F. Eastman, Cornell University, Ithaca, NY, and E. Kohn, Thomson-CSF/DCM, Orsay, FRANCE 594

11:10 a.m.  
25.6 4×4 BIT GaAs DCEL PARALLEL MULTIPLIER, N. Toyoda, T. Terada, K. Kanazawa, S. Shimizu, H. Yamada, and A. Hojo, Toshiba Corporation, Kawasaki, JAPAN 598

11:35 a.m.  
25.7 CAPABILITY OF GaAs DCEL TO HIGH SPEED GATE ARRAY, N. Toyoda, T. Terada, M. Mochizuki, K. Kanazawa, T. Mizoguchi, and A. Hojo, Toshiba Corporation, Kawasaki, JAPAN 602

**SESSION 26: Integrated Circuits—Random Access Memory**

Wednesday, December 15, 9:00 a.m.  
Imperial Room

Co-Chairmen: J.J. Barnes  
K.H. Horninger

9:00 a.m.  
**INTRODUCTION**

9:05 a.m.  
26.1 REDUNDANCY—THE NEW DEVICE TECHNOLOGY FOR CIRCUITS OF THE 19's (Invited Paper), R.J. Smith, Intel Corporation, Santa Clara, CA 608

9:30 a.m.  
26.2 HIGH ISOLATION OF DRAM STORAGE CAPACITORS, D.M. Erb, A. McCombs, and M. Radwin, Advanced Micro Devices Incorporated, Sunnyvale, CA 612

9:55 a.m.  
26.3 A HIGH DENSITY, HIGH PERFORMANCE 1T1 DRAM CELL, A. Mohsen, J. McCollum, R. Breivogel, S. Fu, E. Handy, D. McNelly, and L. Patterson, Intel Corporation, Aloha, OR 616

10:20 a.m.  
26.4 A 55ns 64K DYNAMIC MOS RAM WITH TRIPLE DIFFUSED MOS TRANSISTOR, Y. Nagayama, Y. Ohbayashi, T. Yoshitake, M. Taniguchi, and T. Nakano, Mitsubishi Electric Corporation, Itami, JAPAN 620

10:45 a.m.  
26.5 A NEW VLSI MEMORY CELL USING CAPACITANCE COUPLING, K. Terada, M. Takada, T. Ishijima, S. Kurosawa, and S. Suzuki, Nippon Electric Company, Ltd., Kawasaki, JAPAN 624

11:10 a.m.  
26.6 A SUBTHRESHOLD LOAD ELEMENT FOR HIGH DENSITY STATIC RAM, K.L. Wang, A.H. Shah, H. Shichijo, C. Gossamer, and P.R. Chatterjee, Texas Instruments Incorporated, Dallas, TX 628

11:35 a.m.  
26.7 ALPHA PARTICLE INDUCED CHARGE COLLECTION MEASUREMENTS AND THE EFFECTIVENESS OF REFLECTING BARRIERS ON VLSI MEMORIES, S.W. Fan, A.M. Momen, and T.C. May, Intel Corporation, Aloha, OR 632

**SESSION 27: Solid State Devices—Silicon Field Effect Devices**

Wednesday, December 15, 9:00 a.m.  
Hilton Plaza

Co-Chairmen: C.L. Wilson  
H.N. Yu

9:00 a.m.  
**INTRODUCTION**

9:05 a.m.  
27.1 PHYSICS AND SIMULATION OF SMALL MOS DEVICES (Invited Paper), W. Fichtner, Bell Laboratories, Murray Hill, NJ 638



- 9:30 a.m.  
**272 A GATE LENGTH BURIED CHANNEL SILICON MOSFETS**, R.G. Swartz, R.E. Howard, L.D. Jackel, B. Grubbs, R.W. Epworth, D.M. Tennant, and V.D. Archer, *Bell Telephone Laboratories, Holmdel, NJ* 642
- 9:55 a.m.  
**273 SILICON PERMEABLE BASE TRANSISTORS FABRICATED WITH A NEW SUBMICRON TECHNIQUE**, J.Y. Chu, P. Yee, and R.P. Holmstrom, *GTE Laboratories, Incorporated, Waltham, MA* 646
- 10:20 a.m.  
**274 THE MICROWAVE SILICON PERMEABLE BASE TRANSISTOR**, D.J. Silversmith, D.D. Rathman, N.P. Eptonou, R.W. Mountain, and S.M. Cabral, *M.I.T. Lincoln Laboratory, Lexington, MA* 650
- 10:45 a.m.  
**275 A COMPLETE LARGE AND SMALL SIGNAL CHARGE MODEL FOR AN MOS FIELD EFFECT TRANSISTOR**, R. Conilogue, and C.E. Viswanathan, *University of California, Los Angeles, CA* 654
- 11:10 a.m.  
**276 GATE-CONTROLLED MISIM SWITCH**, C.L. Shieh, S. Wagner, *Princeton University, Princeton, NJ*, L.D. Jackel, and R.E. Howard, *Bell Laboratories, Murray Hill, NJ* 658
- 11:35 a.m.  
**277 CHARACTERIZATION OF 1/f NOISE IN MOS TRANSISTORS**, H. Mochizuki, M. Sakamoto, and Y. Hori, *Nippon Electric Company, Ltd., Kanagawa, JAPAN* 662
- SESSION 28: Integrated Circuit—Bipolar Devices and Modeling** 667  
 Wednesday, December 15, 2000 a.m.  
*Pacific Room*  
 Co-Chairmen: A. Anzai  
 D. Tang
- 9:30 a.m.  
**INTRODUCTION**
- 9:55 a.m.  
**28.1 THE INFLUENCE OF SURFACE TREATMENTS ON THE ELECTRICAL CHARACTERISTICS OF POLY-SILICON EMITTER BIPOLAR TRANSISTORS**, B. Soetewij, P. Ashburn, and A. Cuthbertson, *Southampton University, Hampshire, ENGLAND* 668
- 9:30 a.m.  
**28.2 STATISTICAL MODELING OF SUBMICRON, SHALLOW JUNCTION SELF-ALIGNED BIPOLAR TRANSISTORS**, F.Y. Chang, and S.F. Chu, *IBM Corporation, Hopewell Junction, NY* 672
- 9:55 a.m.  
**28.3 ADVANCED CONCEPTS IN VLSI SCHOTTKY-BARRIER DIODE MODELING**, L.F. Wagner, *IBM Corporation, Hopewell Junction, NY* 676
- 10:20 a.m.  
**28.4 A VLSI MULTIPLE INPUT/OUTPUT ISL GATE DEMONSTRATED IN A 1.25 μm OXIDE-ISOLATED BIPOLAR PROCESS**, T. Yu, P. Roberts, D. Lamb, R. Bell, J. Bosick, N. Zafar, G. Lee, J. Joseph, and D. Prestholdt, *Honeywell Systems and Research Center, Minneapolis, MN*, S. Pal, D. Burbank, H. Vyas, and D. Nielsen, *Honeywell Solid State Electronics Center, Plymouth, MN* 680
- 10:45 a.m.  
**28.5 100 PSEC PL CIRCUITS WITH FIVE-FOLD SELF-ALIGNMENT**, T. Nakamura, K. Nakazato, T. Miyazaki, M. Oshima, T. Okabe, and M. Nagata, *Hitachi Ltd., Tokyo, JAPAN* 684
- 11:10 a.m.  
**28.6 ON THE MONTE CARLO SIMULATION OF BIPOLAR DEVICE**, Y.J. Park, T.W. Tang, and D.H. Navon, *University of Massachusetts, Amherst, MA* 688
- 11:35 a.m.  
**28.7 OVERVIEW OF DEVICE CHARACTERIZATION SOFTWARE FOR VLSI BIPOLAR DEVICES**, O.E. Akcasu, and K.L. Bouknight, and H.C. Nicolay, *Harris Semiconductor, Melbourne, FL* 692

## SESSION 29: Device Technology—Advanced MOS Technologies

- Wednesday, December 15, 1:30 p.m.  
*Continental Ballroom 4-85*  
 Co-Chairmen: R.G. Healderson  
 Y. El-Mansy
- 1:30 p.m.  
**INTRODUCTION**
- 1:35 p.m.  
**29.1 AN OXIDE MASKED P+ SOURCE/DRAIN IMPLANT FOR VLSI CMOS**, A.C. Hui, S.Y. Chiang, and K.M. Cham, *Hewlett Packard Laboratories, Palo Alto, CA* 696
- 2:00 p.m.  
**29.2 HIGH SPEED 1 μm CMOS TECHNOLOGY**, I. Saka, O. Kudo, and H. Yamamoto, *Nippon Electric Company, Ltd., Kanagawa, JAPAN* 702
- 2:25 p.m.  
**29.3 TWIN-TUB CMOS II—AN ADVANCED VLSI TECHNOLOGY**, L.C. Parrillo, L.K. Wang, R.D. Swanson, R.L. Field, R.C. Melin, and R.A. Levy, *Bell Laboratories, Murray Hill, NJ* 706
- 2:50 p.m.  
**29.4 DESIGN AND FABRICATION OF CHANNEL FETTOR 1 μm CMOS TECHNOLOGY**, G.J. Hu, C.Y. Ting, Y. Taur, and R.H. Denard, *IBM Corporation, Yorktown Heights, NY* 710
- 3:15 p.m.  
**29.5 TITANIUM DISILICIDE SELF-ALIGNED SOURCE/ DRAIN AND GATE CMOS TECHNOLOGY**, C.K. Lau, Y.C. See, D.B. Scott, J.M. Bridges, S.M. Perna, and R.D. Davis, *Texas Instruments Incorporated, Dallas, TX* 714
- 3:40 p.m.  
**29.6 A HALF MICRON MOSFET USING DOUBLE IMPLANTED LDD**, S. Ogura, C.F. Cordella, N. Kovalev, J.F. Shepard, and J. Roseman, *IBM General Technology, Hopewell Junction, NY* 718
- 4:05 p.m.  
**29.7 0.1 μm CHANNEL LENGTH MOSFET FABRICATED USING E-BEAM LITHOGRAPHY**, W. Fichtner, R.K. Watts, D.B. Fraser, R.L. Johnston, and S.M. Sze, *Bell Laboratories, Murray Hill, NJ* 722

## SESSION 30: Integrated Circuits—Non-Volatile Memory Devices & Modeling

- Wednesday, December 15, 1:30 p.m.  
*Imperial Room*  
 Co-Chairmen: W. Shedd  
 P. Chatterjee
- 1:30 p.m.  
**INTRODUCTION**
- 1:35 p.m.  
**30.1 HIGH DENSITY 5 VOLT-ONLY COMPATIBLE NON-VOLATILE RAM CELL**, D.G. Guerman, *MOSTEK Corporation, Carrollton, TX* 728
- 2:00 p.m.  
**30.2 AN ADVANCED MNOS MEMORY DEVICE FOR HIGHLY INTEGRATED BYTE-ERASABLE 5V-ONLY EPROMS**, Y. Yatsuda, S. Minami, T. Hagiwara, T. Toyabe, S. Asai, and K. Uchida, *Hitachi Ltd., Tokyo, JAPAN* 732
- 2:25 p.m.  
**30.3 CELL MODEL FOR EPROM FLOATING GATE MEMORIES**, P. Sucu, B. Cox, D. Rinerson, and S. Cagnina, *Advanced Micro Devices Incorporated, Sunnyvale, CA* 737
- 2:50 p.m.  
**30.4 EPROM CELL WITH HIGH GATE INJECTION EFFICIENCY**, M. Kamiya, Y. Kojima, Y. Kato, K. Tanaka, *Daini-Seikasha Company, Ltd., Matsudo, JAPAN*, and Y. Hayashi, *Electrotechnical Laboratory, Nukhari-gun, JAPAN* 741

3:15 p.m.  
305 NONUNIFORM DISPLACEMENT OF MOSFET CHANNEL LINCHOFF, S.G. Chamberlain, A. Husain, *University of Waterloo, Ontario, CANADA*, and F.H. Gaenslen, IBM Thomas J. Watson Research Center, Yorktown Heights, NY 745

3:40 p.m.  
306 ELECTRON TUNNELING IN NON PLANAR FLOATING GATE MEMORY STRUCTURE, R.E. Ellis, H.A.R. Wegener, and J.M. Caywood, MICOR Incorporated, Milpitas, CA 749

4:05 p.m.  
307 EFFECTS OF AVALANCHE INJECTION CURRENTS ON THE ENDURANCE OF SIMOS DEVICES, C.T. Sah, J.Y.C. Sun, and J.J.T. Tsai, *University of Illinois, Urbana, IL* 753

### SESSION 31: Solid State Devices—Novel Devices & Technologies

Wednesday, December 15, 1:30 p.m.  
Hilton Plaza

Co-Chairmen: M.C. Driver  
D.E. Ackley

1:30 p.m.  
INTRODUCTION

1:35 p.m.  
31.1 MATERIALS SCIENCE OF JOSEPHSON JUNCTIONS (Invited Paper), M.R. Beasley, *Stanford University, Stanford, CA* 758

2:00 p.m.  
31.2 RESISTOR COUPLED JOSEPHSON LOGIC FULL ADDER CIRCUIT, J. Song, T. Yoshida, S. Takara, and H. Abe, *Nippon Electric Company, Ltd., Kawasaki, JAPAN* 762

2:25 p.m.  
31.3 InGaAs/InAlAs HETEROJUNCTION LATERAL PNP TRANSISTORS, K. Tabatabaie-Alavi, A.N.M.M. Choudhury, J. Vitek, N. Slater, C.G. Fonstad, *Massachusetts Institute of Technology, Cambridge, MA*, K. Alavi, and A.Y. Cho, *Bell Laboratories, Murray Hill, NJ* 766

2:50 p.m.  
31.4 NOTCHED InP PLANAR TRANSFERRED ELECTRON OSCILLATORS, S.C. Binari, P.E. Thompson, *Naval Research Lab., Washington, DC*, H.L. Grubin, *Scientific Research Associates, Inc., Glastonbury, CT* 770

3:15 p.m.  
31.5 X-BAND SELF-ALIGNED GATE ENHANCEMENT MODE InP MISFETs, T. Itoh, and K. Ohara, *Nippon Electric Company, LTD., Kawasaki, JAPAN* 774

3:40 p.m.  
31.6 MEASUREMENT OF ELECTRON DRIFT VELOCITY IN COMPOSITIONALLY GRADED AlGa<sub>1-x</sub>As BY TIME RESOLVED OPTICAL PICOSECOND REFLECTIVITY, B.F. Levine, W.T. Tsang, C.G. Bethea, and F. Capasso, *Bell Laboratories, Murray Hill, NJ* 778

4:05 p.m.  
31.7 HIGH FIELD CONDUCTION MECHANISMS IN POLY-CRYSTALLINE SILICON RESISTORS, N.C.C. Lu, IBM T.J. Watson Research Center, Yorktown Heights, NY, and C.Y. Lu, M.K. Lee, *Institute of Electronics, National Chiao-Tung University*, and G. Chang, *Integrated Circuits Laboratory, Stanford University, Stanford, CA* 781

### LATE NEWS

785

## HIGH-VOLTAGE DMOS AND PMOS IN ANALOG IC'S

A.W. Ludikhuize

Philips Research Laboratories  
Eindhoven - The Netherlands

## ABSTRACT

A lateral 300V DMOS device is described which can be integrated in a standard bipolar IC process. The device, applicable as a high voltage source follower for analog circuits, is based upon the "double-acting resurf" principle; a modification with an interrupted p-top layer or with a stepped field plate is used. The p-layer improves the interconnection-induced breakdown and can be used in the extended drain of a 280 V PMOST.

## INTRODUCTION

For functions like driving transducers or CRT's and for analog switches, high voltage analog stages of over 250 V may be needed on the chip. Vertical bipolars are less suitable because of the required thick epi-layers and even integration of vertical DMOS devices in a standard IC process is rather difficult. High voltage lateral MOS devices of over 500 V, using thin layer extended drain or "resurf" techniques (1-3), can easily be incorporated, but a high voltage source follower is impossible. Source followers using lateral DMOS devices and 25-30  $\mu\text{m}$  epi have been reported (4); here 200 V is considered the limit for junction isolated devices because of deep isolation diffusions and parasitic bulk and surface effects (5). Recently a "double-acting resurf" technique has been reported (6); compared to "resurf" as mentioned above, it not only offers better lateral conduction but also prevention of substrate punch-through in follower applications. Owing to a higher doping content of the n-layer (about  $2 \cdot 10^{12} \text{ cm}^{-2}$ ), the depletion layer at source (back gate)-to-substrate breakdown does not extend to the surface diffusion (as shown by the left-hand shaded area in fig. 1) and no punch-through occurs. At high voltage on the n-drain with the other terminals grounded, a high field would occur at the source edge. By using a p-top layer, depletion of the p-layer is obtained from the top and the bottom (right-hand shaded areas in fig. 1) causing a

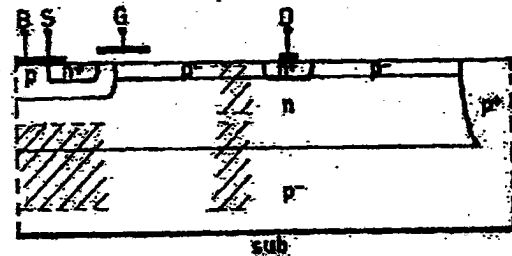


Fig. 1. A double-acting resurf structure. smooth voltage decrease over the lateral distance between source and drain; at high drain voltage this p-top layer has to be depleted too. The effect was demonstrated on JFET and lateral bipolar devices (6); the p- and n-layers were optimized at  $0.5 \cdot 10^{12} \text{ cm}^{-2}$  and  $1.8 \cdot 10^{12} \text{ cm}^{-2}$  respectively.

## LATERAL DMOST

For proper functioning of a lateral DMOST (LDMOST), the design of Fig. 1 has to be adapted. In fig. 2 a window is shown, made locally in the p-layer at the source side; electrons from the gate-controlled surface channel now pass through a vertical JFET which limits the current capability and increases the on-resistance. The window dimensions are therefore a compromise between on-resistance and breakdown.

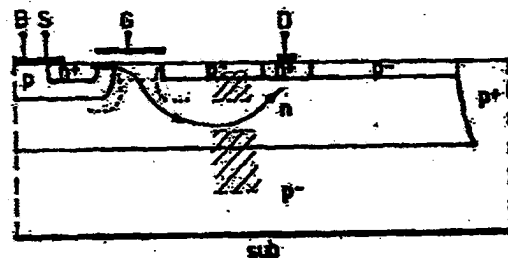


Fig. 2. LDMOST with interrupted p-layer.

Instead of a p-top layer also a stepped field plate, connected to gate or source, can be applied in order to obtain depletion from the surface, as shown in fig. 3.

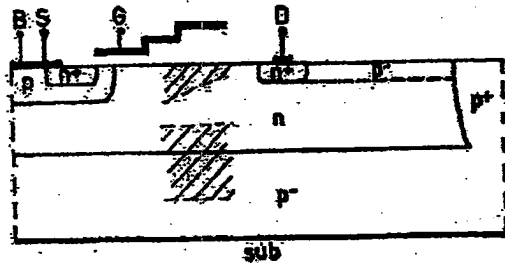


Fig. 3. LDMOST with stepped field plate.

The pinching effect on the n layer is much less, lowering the breakdown voltage, but now the entire epi-layer with local accumulation contributes to a low on-resistance.

Computer calculations using our 2D Poisson program "Semmy" were performed on the structure depicted in fig. 4 for several combinations of p-layer and field plates, cf. table 1. A  $15 \mu\text{m}$   $5\mu\text{m}$  n-type epi-layer as used in a 50-60 V standard bipolar process is applied on a  $30\Omega\text{cm}$  p-substrate. The  $3 \mu\text{m}$  p-layer, assumed without a window here, has a net dose of  $1.6 \cdot 10^{12} \text{ cm}^{-2}$ ; this high value improves the current capability of an extended drain PMOST as will be discussed later on,

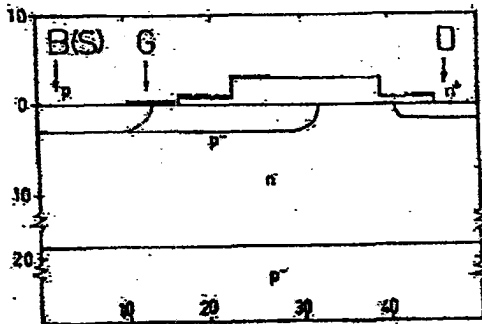


Fig. 4. LDMOST structure; dimensions in  $\mu\text{m}$ .

but delays pinch off and requires the p-layer to be withdrawn from the n drain in order to prevent low breakdown values. The gate-oxide is  $8.1 \mu\text{m}$ ; the field plates (etched) step on  $0.8$  and  $3.0 \mu\text{m}$  oxide. The punchthrough voltage to the substrate is calculated to be  $600\text{V}$ ; spreading of epi-dope and thickness may decrease this value to  $300 \text{ V}$ .

In figs. 5 and 6 equipotential and equipotential lines at  $300 \text{ V}$  drain voltage are shown for a device with a p-layer; the

co-operation of top and bottom depletion is visible on the left in fig. 5. The highest field of  $23.2 \text{ V}/\mu\text{m}$ , obtained at the p-diffusion curvature, does not cause breakdown (avalanche integral  $<1$ ).

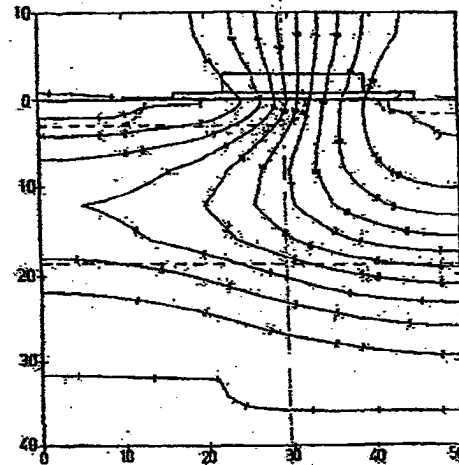


Fig. 5. LDMOST equipotential lines at  $V_{d-s} = 300\text{V}$ ; per step  $30\text{V}$ , step 1=0V.

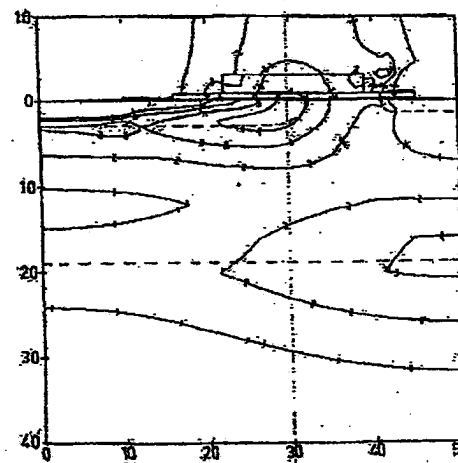


Fig. 6. LDMOST equipotential lines at  $V_{d-s} = 300\text{V}$ ; per step  $5\text{V}/\mu\text{m}$ , step 1= $5\text{V}/\mu\text{m}$ .

Table 1  $E_{\text{max}}$  (in  $\text{V}/\mu\text{m}$ ) at  $V_{d-s}=300\text{V}$ ; epi, p-layer and field plates (F.P.) as in fig. 4.

substr.	p-	F.P.	$E_{\text{max}5f}$	B.V.	$E_{\text{max}ox}$
n	yes	yes	32.0	$<300$	56
p-	no	no	63.5	$<300$	172
p-	yes	no	23.2	$>300$	22.7
p-	no	yes	28.7	$>300$	95
p-	yes	yes	24.5	$>300$	35



Fig. 7. shows an actual device with a stepped field plate connected to the source; the layout corners are bevelled. At the connection of the polysilicon gate the field plate had to be interrupted as single-layer metallization is used and a local p-layer is applied. The active gate width is 500  $\mu\text{m}$ , the channel length is approx. 2.0  $\mu\text{m}$ . The drain surrounds the back gate and prevents parasitic PMOS action from back gate to isolation when the source is at high voltage. As crossing interconnection over shallow  $n^+$  shows only 200V breakdown on 3.0  $\mu\text{m}$  oxide, the shallow  $n^+$  drain has been locally omitted underneath this metallization. A collector wall diffusion

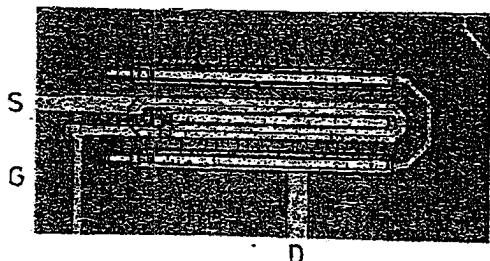


Fig. 7. LDMOST for 300V; gate and source with field plate in the centre,  $n^+$  drain 3/4 around as a stopper; drain pitch 90  $\mu\text{m}$ .

or a buried polysilicon field shield can be used here; this way a breakdown >300 V is obtained. At the isolation diffusion edge a p-layer is applied (withdrawn from the  $n$  drain), which improves breakdown noticeably in the case of crossing (drain) interconnection and avoids walk-out phenomena below 300V.

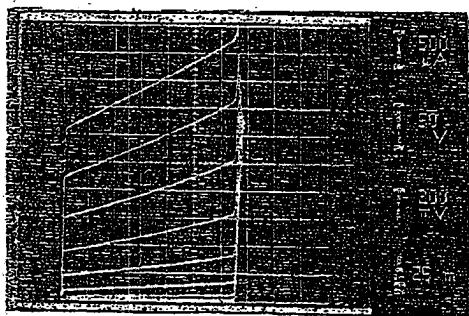


Fig. 8. LDMOST BV drain-to-source; the substrate is connected to the source.

A source-to-substrate breakdown of over 300V was obtained limited by the drain-to-isolation distance. Drain-to-source breakdown (substrate is at source potential) is shown in fig. 8 to be over 300V; breakdown generally occurs at the bevelled

back gate corners.

Fig. 9 shows the low-voltage on-characteristics.  $V_T$  is about 2.4V and  $\beta_o = 16 \mu\text{A/V}^2$ ;  $R_{on}$  is 300  $\Omega$  corresponding with 6.7  $\Omega/\text{mm}$  for the active area. Owing to partial depletion of the epi-layer,  $R_{on}$  increases at 300 V s-sub to 450  $\Omega$  and  $I_{on}$  (10V d-s) becomes 18mA. For a variant according to fig. 2 with a p-ring and 10  $\mu\text{m}$  local windows  $R_{on}$  was found to be 450-600  $\Omega$ .

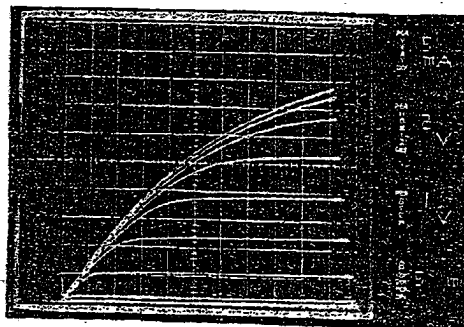


Fig. 9. LDMOS on-characteristics.

Experiments in plastic encapsulation showed good stability in dry ambient at 150°C. In wet ambient instabilities are sometimes observed at the drain. Simulation with a field plate at  $V_{surf}$  on 1  $\mu\text{m}$  nitride on top of the structure indicated the drain configuration of fig. 4 to be poor; a field plate overlapping the  $n^+$  drain edge is sufficient.

#### EXTENDED DRAIN PMOST

In the same process a complementary high-voltage extended drain PMOST (EPMOST) has been made; the extension is pinched between the epi-layer and a stepped field plate connected to source or gate (cf. ref. 7). For better gradual pinching and less early effect in the PMOS channel, a buried  $n^+$  layer is applied locally as shown in fig. 10. Source and back gate are

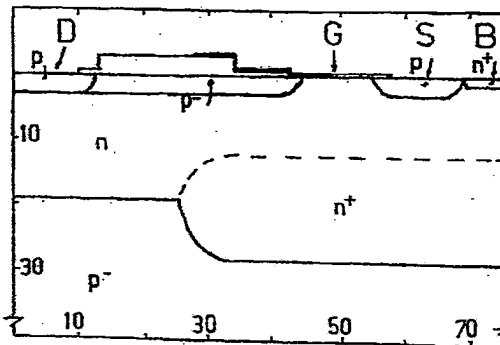


Fig. 10. Extended drain PMOST structure.



situated on the right, drain and p- extension on the left. The effective channel length is about  $11\ \mu\text{m}$ , but lower values with more Early-effect are possible. A computer calculation with 300V on source and gate shows equipotential and equi-field lines (figs. 11 and 12); the maxi-

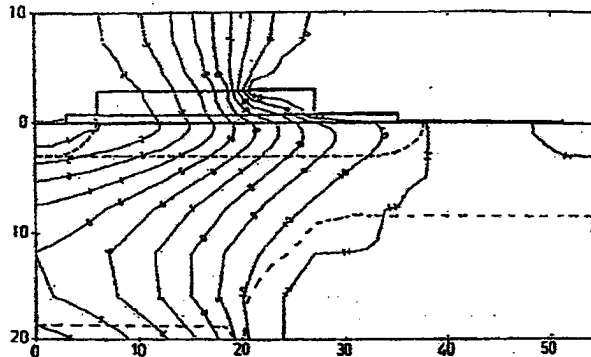


Fig. 11. EPMOST equipotential lines at V s, g-d, sub=300V; per step 30V, step 1=0V.

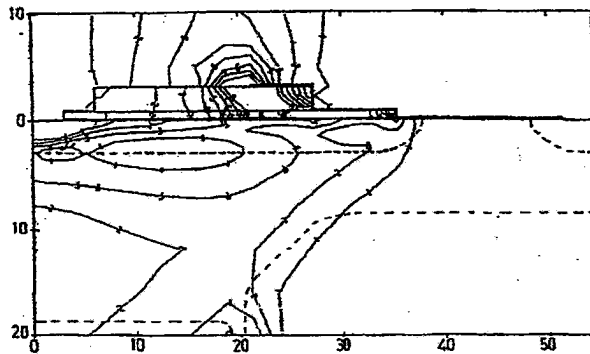


Fig. 12. EPMOST equi-field lines at V s, g-d, sub=300V; per step 5V/ $\mu\text{m}$ , step 1=5V/ $\mu\text{m}$ .

mum field of 23V/ $\mu\text{m}$  does not cause breakdown. An actual EPMOST is shown in fig. 13; the p drain is in the centre and the n<sup>+</sup> backgate contact on the outside of the de-

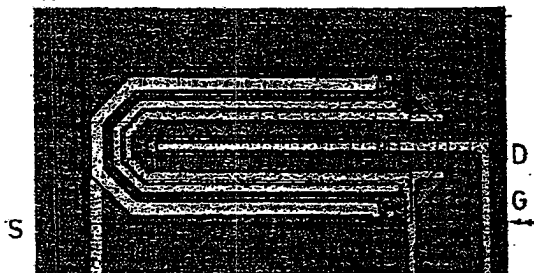


Fig. 13. EPMOST with central drain and gate, source and back gate 3/4 around; the n<sup>+</sup> back gate acts as a stopper; scale as fig. 7.

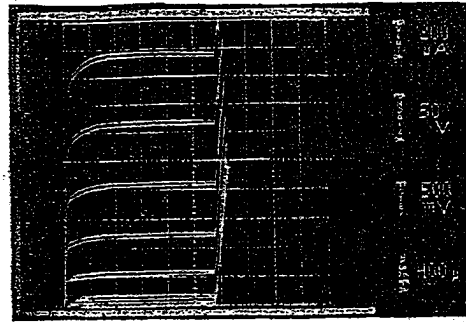


Fig. 14. EPMOST BV drain-to-source; the substrate is connected to the drain.

vice acts as a stopper for parasitic PMOS action.

The measured drain-to-source breakdown is shown in fig. 14 to be 280V; this breakdown occurs at the small-radius end of the drain. The active gate width is about 550  $\mu\text{m}$ ;  $V_t = 1.5\text{V}$ ,  $g_m \text{ max (10V, } g_{ds}) = 1.4\text{mA/V}$  and  $\theta_{ds} = 7\mu\text{A/V}^2 \cdot \text{R}$  is 900  $\Omega$ , corresponding with 30  $\Omega/\text{mm}^2$  for the active area.

#### CONCLUSION

By using a modification of the "double-acting resurf" principle, a lateral DMOST for 300V analog applications can be integrated with standard bipolar components. The use of a p- implanted layer allows interconnections to over 300V on 3  $\mu\text{m}$  oxide. The same p-layer has been used in an extended drain PMOST of 280V.

#### ACKNOWLEDGEMENT

The author wishes to thank his colleagues for their stimulating co-operation and particularly W. Ruis and R. Bonne for preparation of the samples.

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